# CLAIMS

1. A receiver including an analog Barker detector, comprising:

digital processing logic having a receive signal input for processing digital baseband signals and having a power activation input for receiving a detection signal;

a radio that receives and converts radio frequency (RF) signals into analog baseband signals, said radio comprising:

a Barker matched filter coupled to receive said analog baseband signals;

an envelope detector, coupled to said Barker matched filter;

a peak detector, coupled to said envelope detector; and

a counter circuit, coupled to said peak detector, that detects Barker signals and that provides said detection signal; and

an analog-to-digital converter (ADC) that converts said analog baseband signals into said digital baseband signals.

2. The receiver of claim 1, wherein said digital processing logic is powered down between signal acquisitions and powers up in response to said detection signal.

3. The receiver of claim 1, wherein said ADC includes a power activation input receiving said detection signal and is powered down between signal acquisitions and powers up in response to said detection signal.

4. The receiver of claim 1, wherein said radio performs direct conversion and further includes first order DC correction loops using up/down counters as feedback integrators.

5. The receiver of claim 1, wherein said Barker matched filter comprises:

a track and hold stage having an input receiving said analog baseband signals and an output; and

a Barker correlator having an input coupled to said output of said track and hold stage and an output coupled to said envelope detector.

6. The receiver of claim 5, wherein said track and hold stage comprises:

a sample circuit that samples said analog baseband signals and that provides corresponding voltage samples;

a converter that converts each voltage sample to a sample current; and

a plurality of matched current generator stages, coupled to said converter, that converts each said sample current into a plurality of matched AC currents.

7. The receiver of claim 6, wherein each of said plurality of matched current generator stages comprises a current mirror and a slaved current source.

8. The receiver of claim 6, wherein a first of said plurality of matched current generator stages is coupled to a DC offset loop.

9. The receiver of claim 5, wherein said Barker correlator comprises:

a plurality of analog multiply-accumulate (MAC) cells, coupled to said track and hold stage, that collectively performs parallel Barker matched filtering in overlapped filter windows; and

a switched-capacitor (S-C) charge summer and reset circuit having an input coupled to said Barker correlator and an output coupled to said envelope detector.

10. The receiver of claim 9, wherein each of said plurality of analog MAC cells comprises a plurality of capacitors and switches that accumulate weighted current samples over a predetermined filter cycle.

11. The receiver of claim 1, wherein said envelope detector comprises:

a plurality of track and latch comparators;

decode logic coupled to said plurality of track and latch comparators; and

a switched-capacitor charge redistribution summing amplifier coupled to said decode logic.

12. The receiver of claim 1, wherein said peak detector averages Barker correlator filter output samples, derives a dynamic threshold value, and compares said dynamic threshold value with Barker correlator filter output samples.

13. The receiver of claim 1, wherein said peak detector comprises:

a low pass filter (LPF) that averages envelope output samples and that provides a threshold signal; and

a comparator that compares said threshold signal with said envelope output samples.

14. The receiver of claim 13, wherein said LPF incorporates selectable bandwidth and is initially set in a high bandwidth mode during initial acquisition and re-acquisition of noise floor, and is switched to a low bandwidth mode for tracking and signal detection.

15. The receiver of claim 14, wherein said LPF further incorporates a quench mode during which a previously unknown signal state is erased and re-initialized to an expected noise floor value.

16. The receiver of claim 13, further comprising a multiple tap moving average FIR filter coupled between said envelope detector and said peak detector.

17. The receiver of claim 1, wherein said counter circuit comprises two counters that are each reset periodically in a staggered fashion for overlapping windows and an OR circuit coupled to outputs of said two counters.

18. The receiver of claim 1, wherein said counter circuit comprises:

a plurality of overlapped window counters coupled in parallel and having a plurality of outputs; and

decision logic coupled to said plurality of outputs of said plurality of overlapped window counters.

19. The receiver of claim 18, wherein said plurality of overlapped window counters are organized into a pair of parallel enabled banks, each bank comprising a plurality of staggered counters, and each bank reset by approximately half a predetermined detection interval.

20. The analog Barker detector of claim 18, wherein said decision logic comprises OR logic.